奇美電子 CHIMEI INNOLUX

PRODUCT SPECIFICATION

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V420H2

SUFFIX: LH2

Customer: LGE

APPROVED BY SIGNATURE

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	Apple Wen

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Apr. 06, 2010	All	All	The Approval Specification was first issued.
Ver. 2.1	May.14, 2010	27	6.2	LGE request T3 Spec to be corrected as : 0≦T3 ; T2 Spec to be corrected as : 0≦T2≦150ms

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H2-LH2 is a 42″ TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G (8-bit+Hi-FRC). The C-balance board module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (5000:1)
- Fast response time (Gray to gray average 6.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100/120 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02″ diagonal)	mm	(1)
Bezel Opening Area	939 (H) x 531 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	982.0	983.0	984.0	mm	(1), (2)
	Vertical (V)	575.0	576.0	577.0	mm	
	Depth (D)	34.1	35.1	36.1	mm	
Weight		-	9700	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

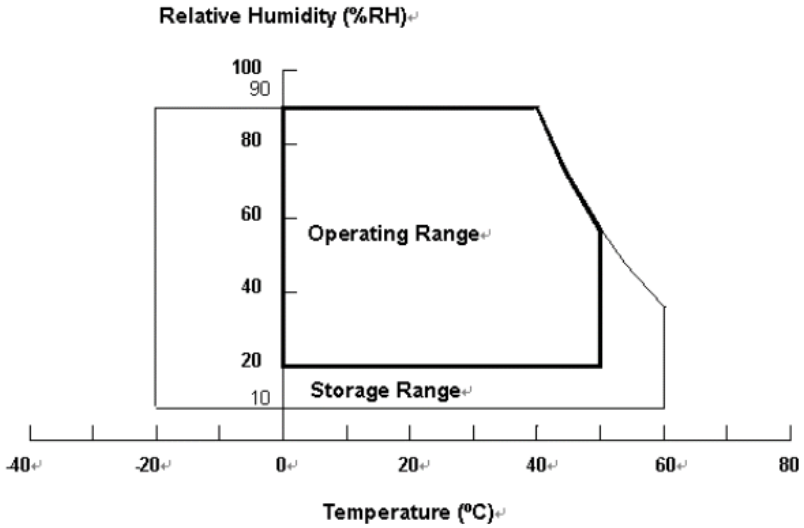
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

3. ELECTRICAL CHARACTERISTICS

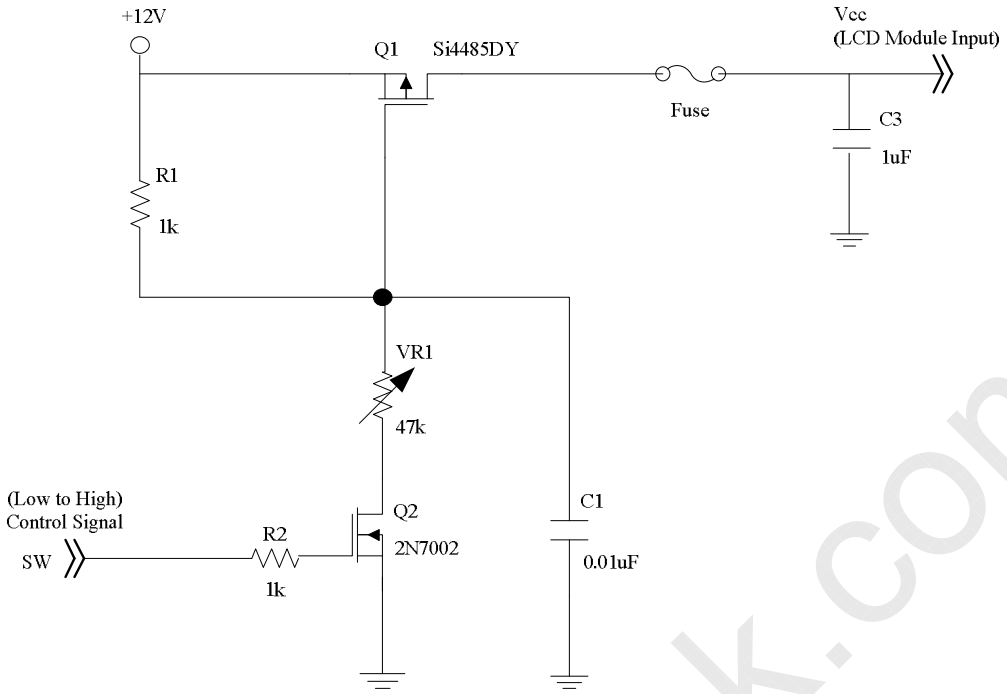
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

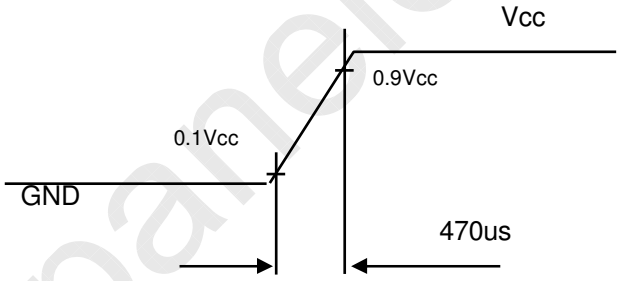
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	4.25	A	(2)
Power Supply Current	White Pattern	—	—	1.29	—	A	(3)
	Horizontal Stripe	—	—	1.37	1.78	A	
	Black Pattern	—	—	0.55	—	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

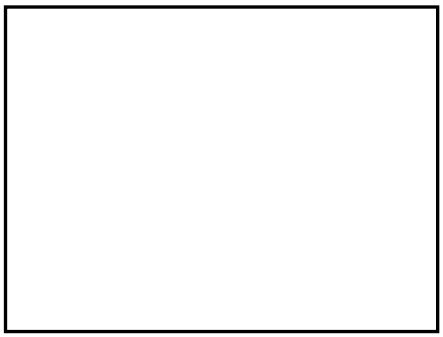


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

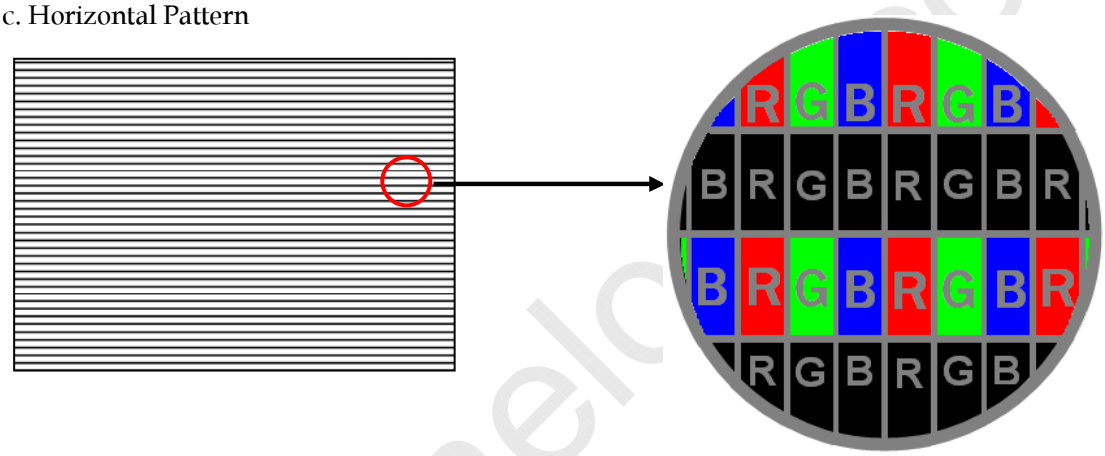


Active Area

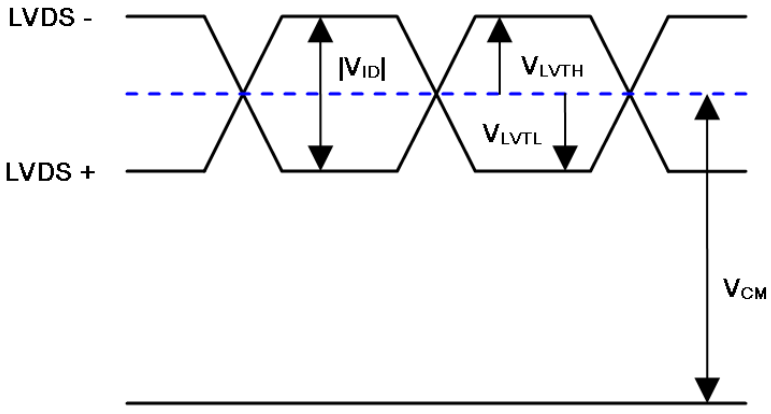
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	VL	-	1090	-	V_{RMS}	
Lamp Current	IL	10.0	10.5	11.0	mA_{RMS}	
Lamp Turn On Voltage	VS	-	-	(1600)	V_{RMS}	Ta = 0 °C
		-	-	(1300)	V_{RMS}	Ta = 25 °C
Operating Frequency	FL	35	-	70	KHz	
Lamp Life Time	LBL	50,000	-	-	Hrs	

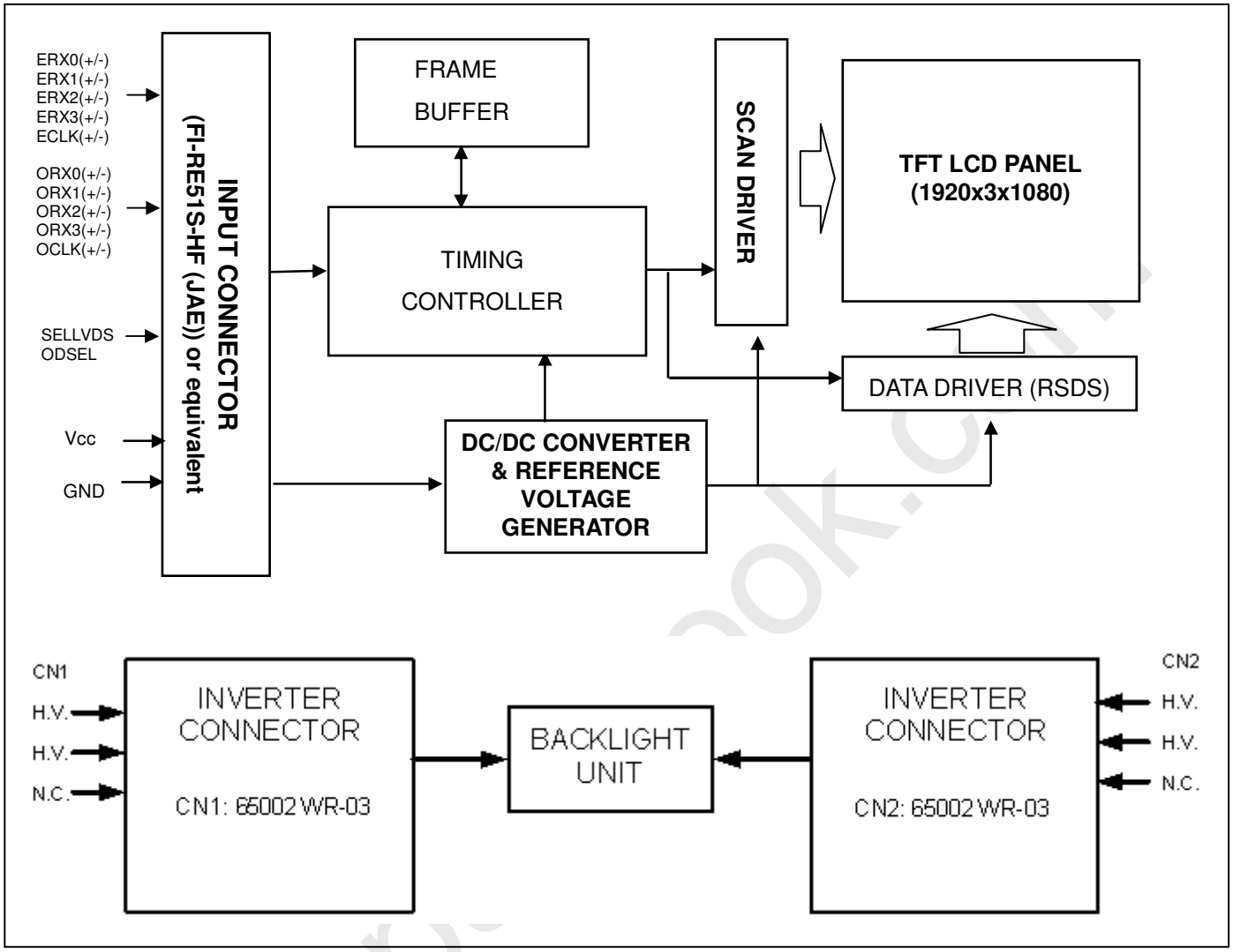
3.2.2 ELECTRICAL SPECIFICATION

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
BL Lamp Voltage	V_{BL}	-	1090	-	V_{RMS}	Half lamp voltage +capacitor voltage
BL Lamp Current	I_{BL}	120	125	130	mA_{RMS}	12 lamps
BL total Power			130	142	W	
Lamp Turn On Voltage	V_S	-	-	(1600)	V_{RMS}	Ta = 0 °C
		-	-	(1300)	V_{RMS}	Ta = 25 °C
Striking time	St			2	sec	
Operating Frequency	F_{BL}	45	48	51	KHz	
Lamp Type	-	Straight Type			-	-
Number of Lamps	-	12			pcs	
Type of current balance		C balance				
Capacitor value	-	-	27	-	pF	

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 1 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	

29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2 Connector Pin Assignment (FI-RE41S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	N.C.	No Connection	(1)

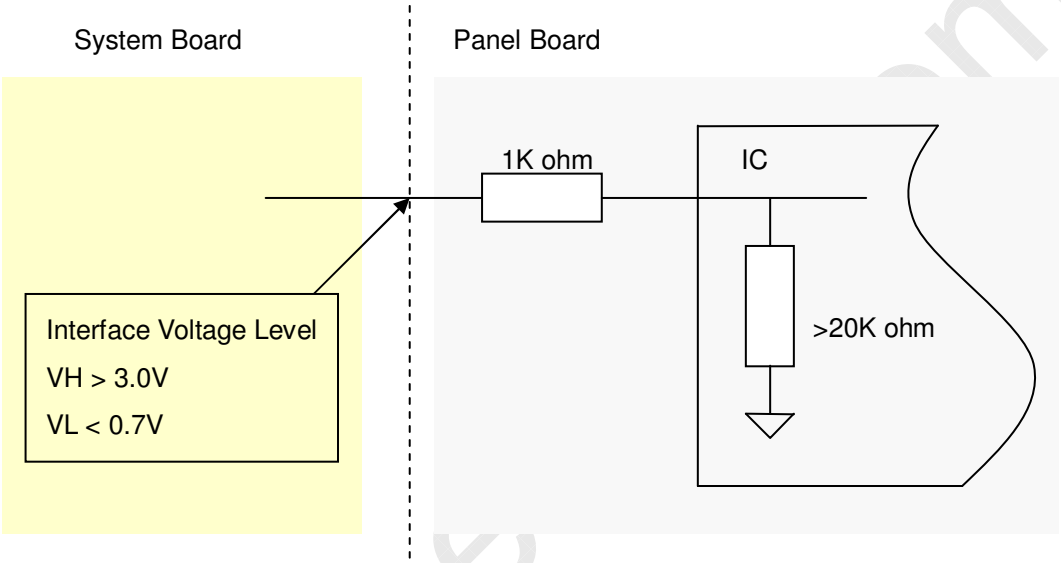
8	N.C.	No Connection	(1)
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	(1)
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	

39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V : JEIDA Format ； Low= connect to GND or Open : VESA Format.

Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.



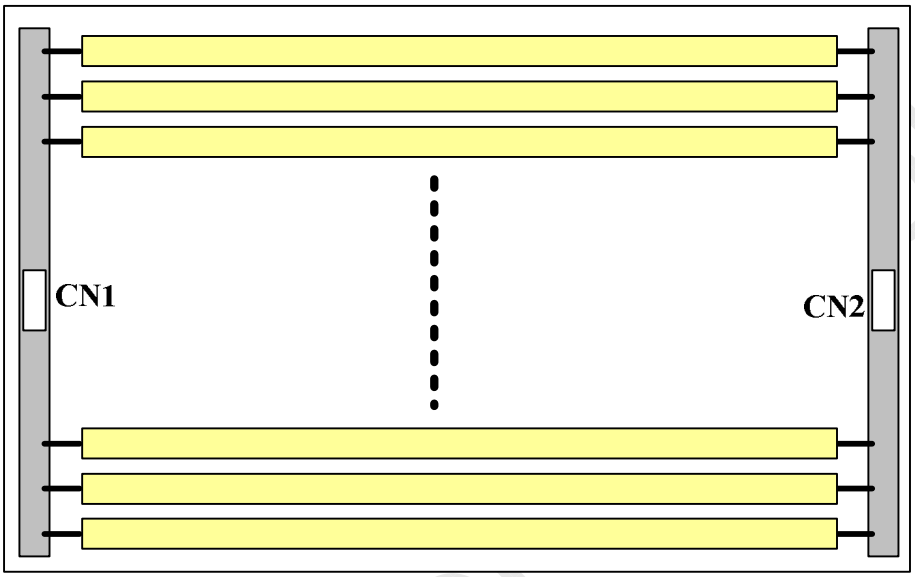
Note (4) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

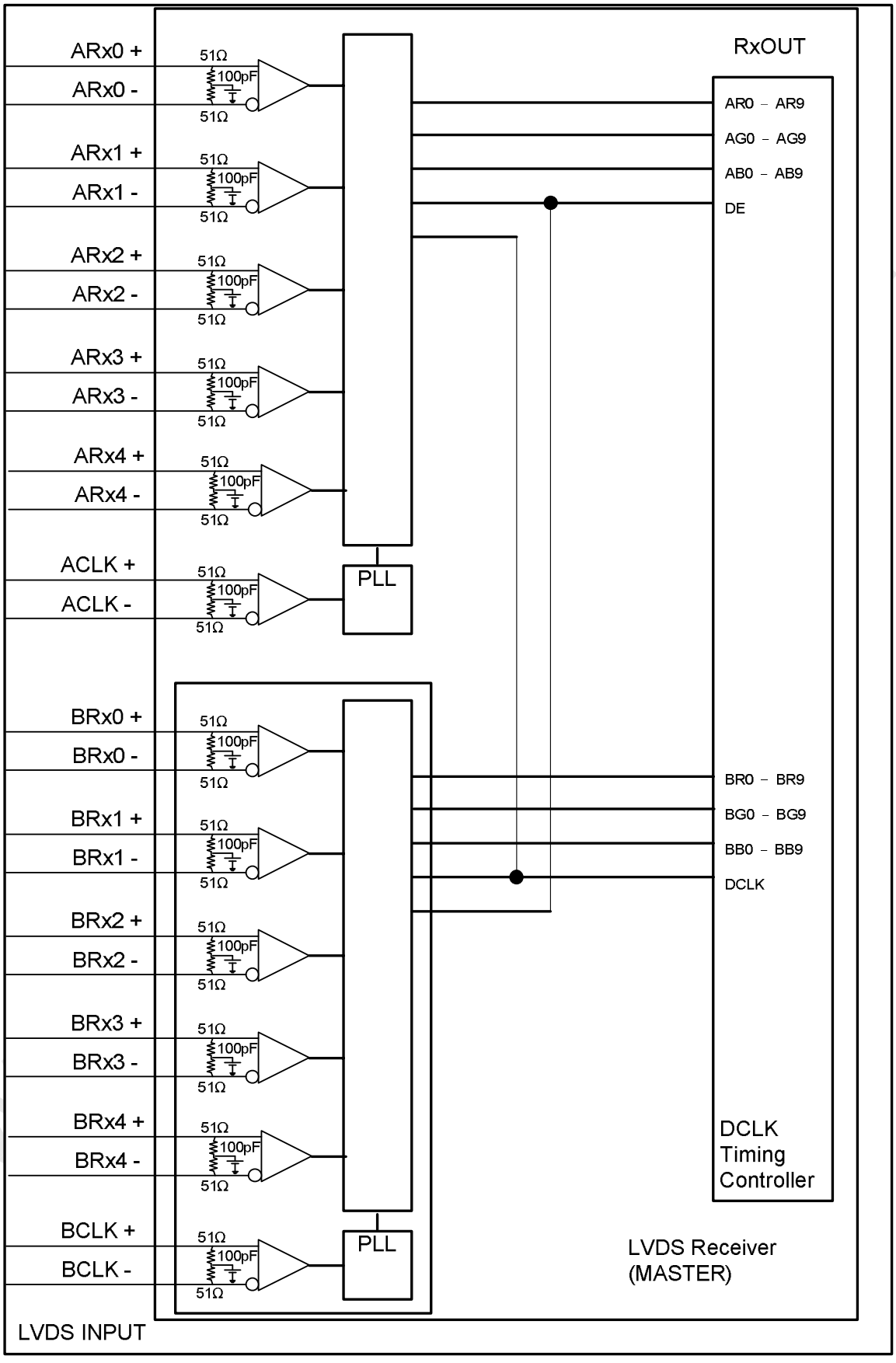
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

Pin	Name	Description	Wire Color
1	HV	High Voltage	White
2	HV	High Voltage	Pink



5.3 BLOCK DIAGRAM OF INTERFACE



AR0~AR9	First pixel R data	BR0~BR9	Second pixel R data
AG0~AG9	First pixel G data	BG0~BG9	Second pixel G data
AB0~AB9	First pixel B data	BB0~BB9	Second pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

CR0~CR9	Third pixel R data	DR0~DR9	Foruth pixel R data
CG0~CG9	Third pixel G data	DG0~DG9	Fourth pixel G data
CB0~CB9	Third pixel B data	DB0~DB9	Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

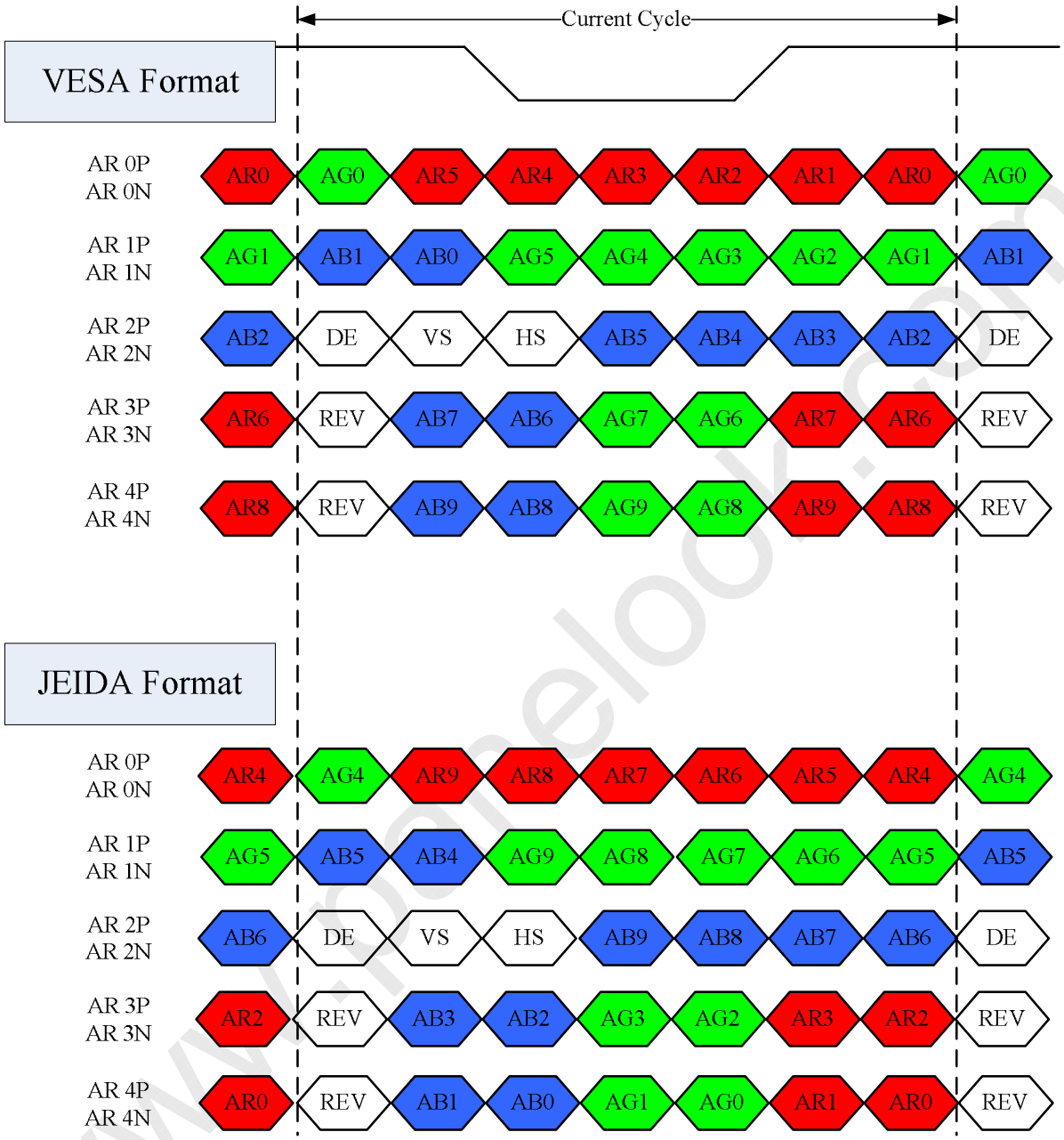
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSV : Reserved

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color.The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Gray	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	TBD	100	TBD	Hz	(6)
		F_{r6}	TBD	120	TBD	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	—
	Blank	Thb	60	70	95	Tc	—

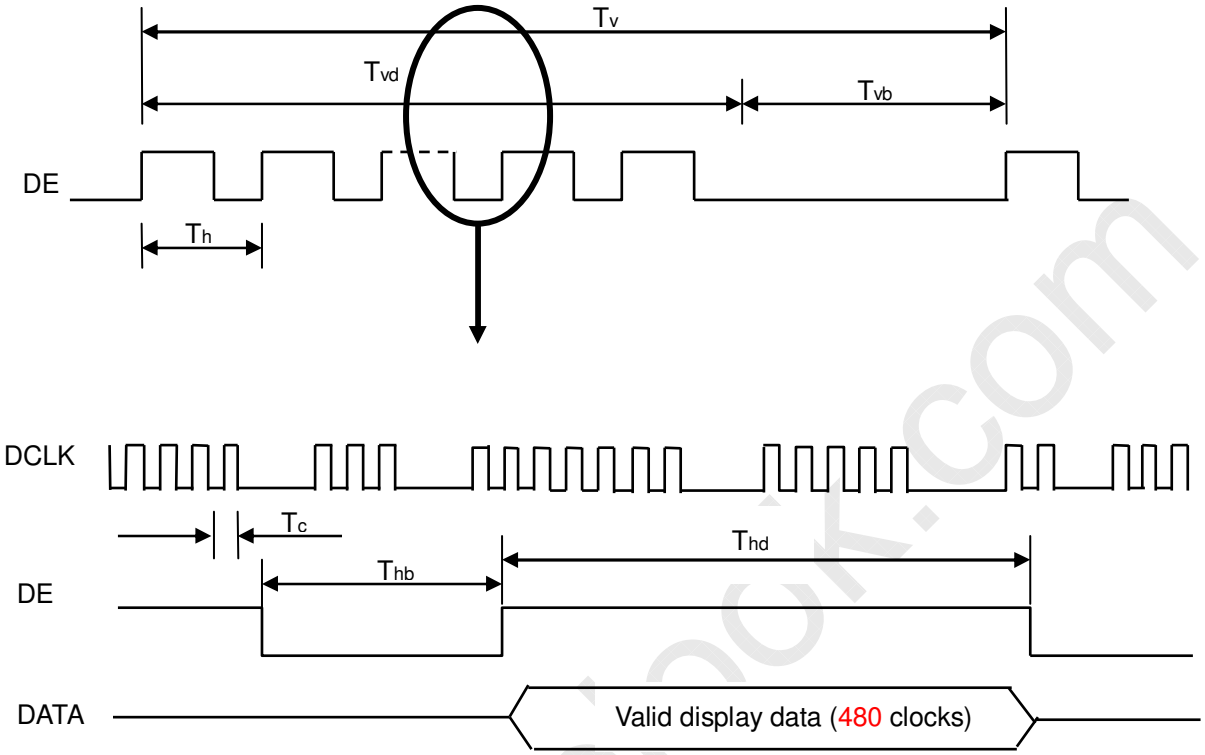
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

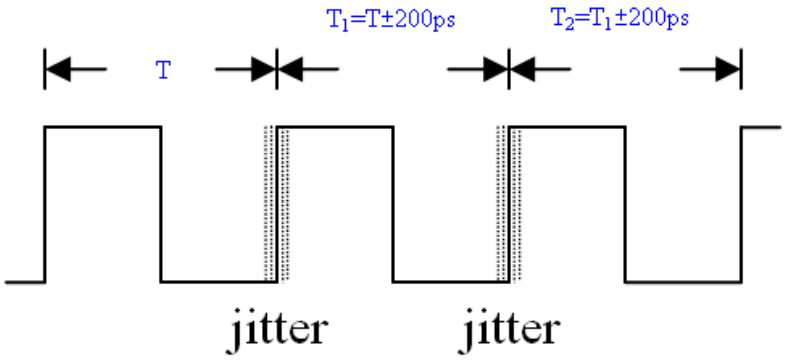
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

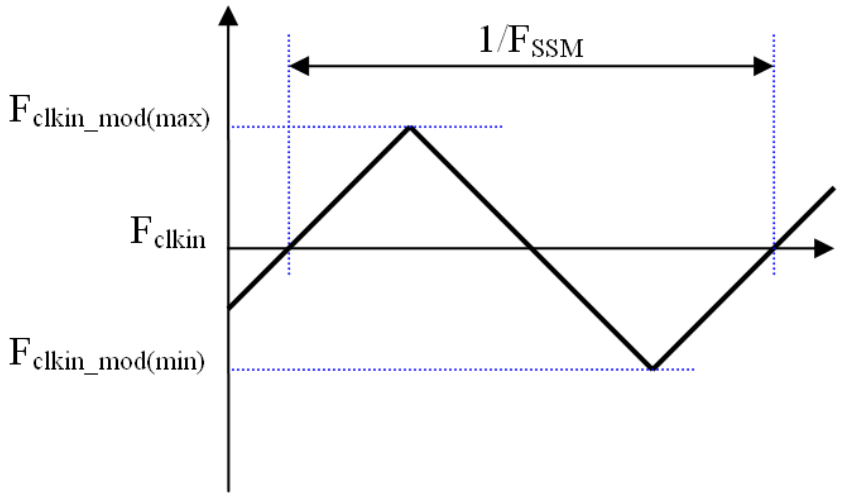
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

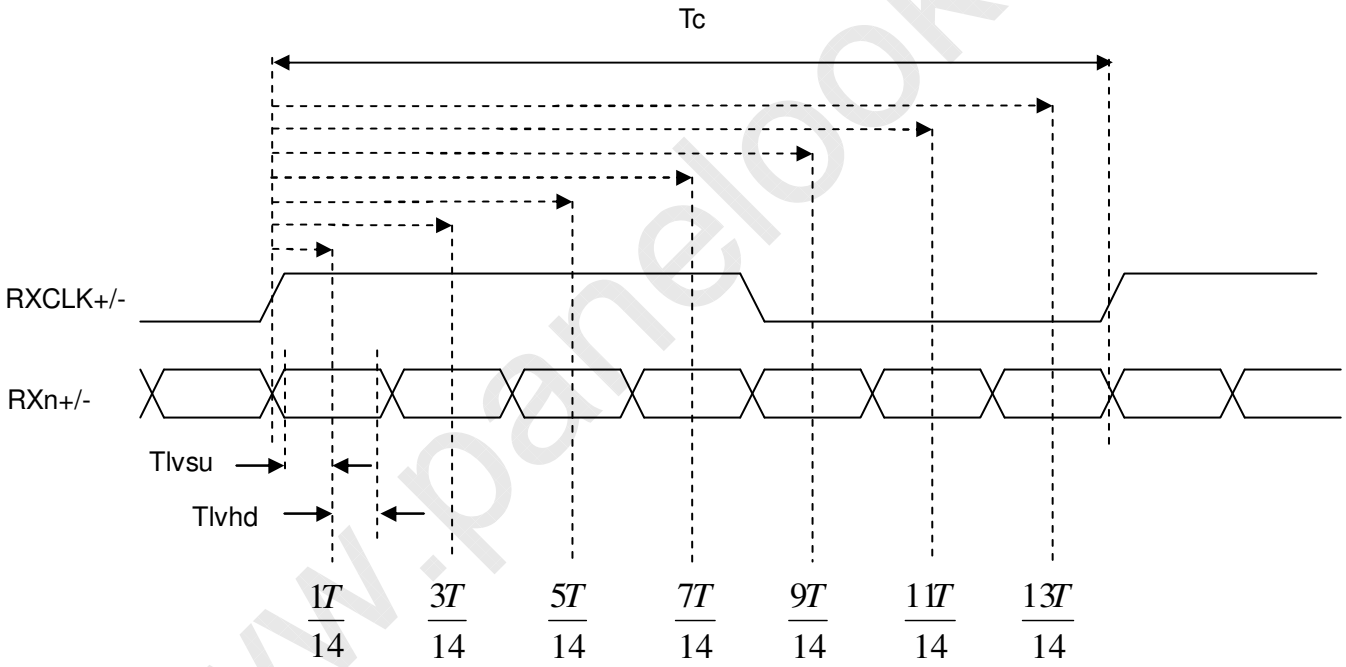


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

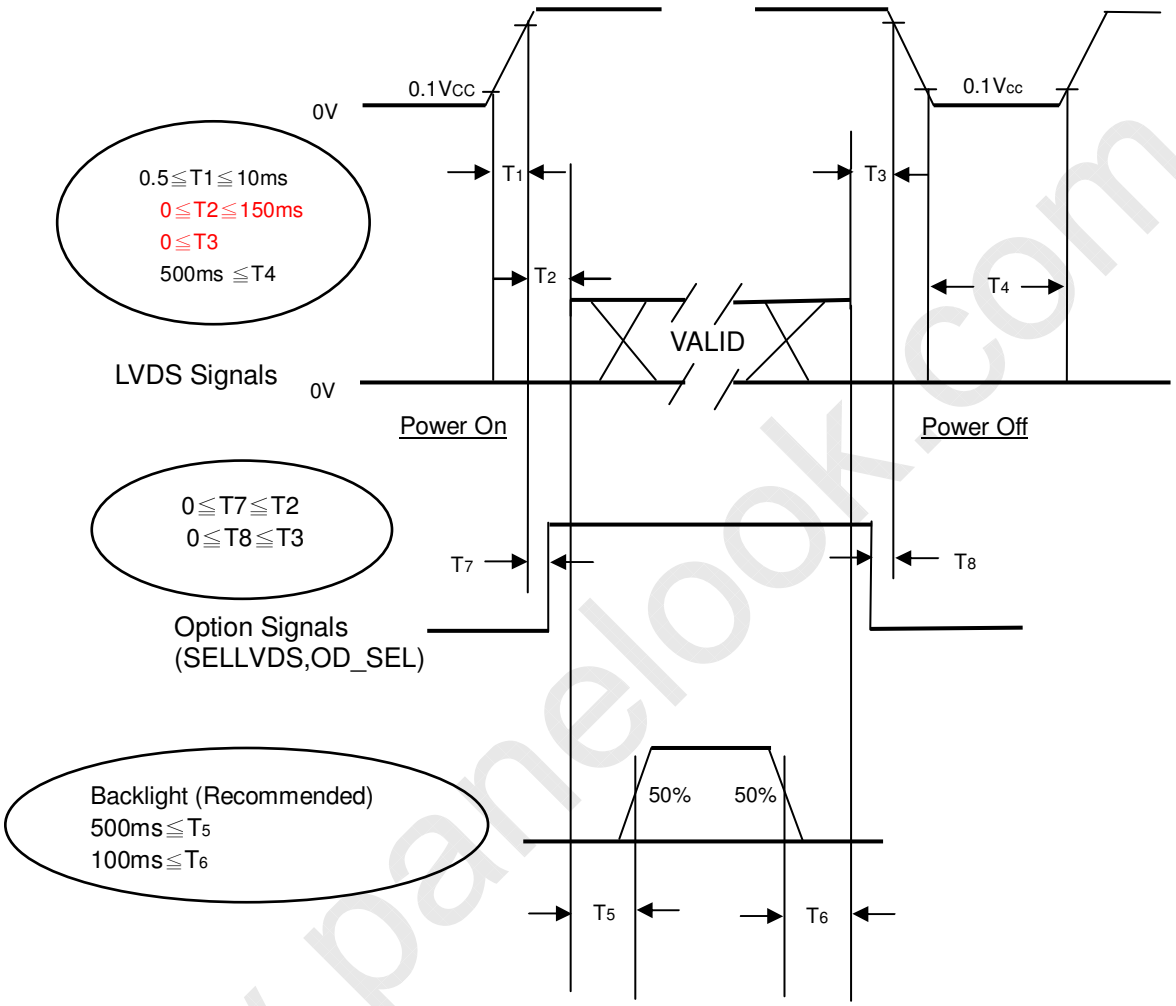


Note (6) : (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 °C)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

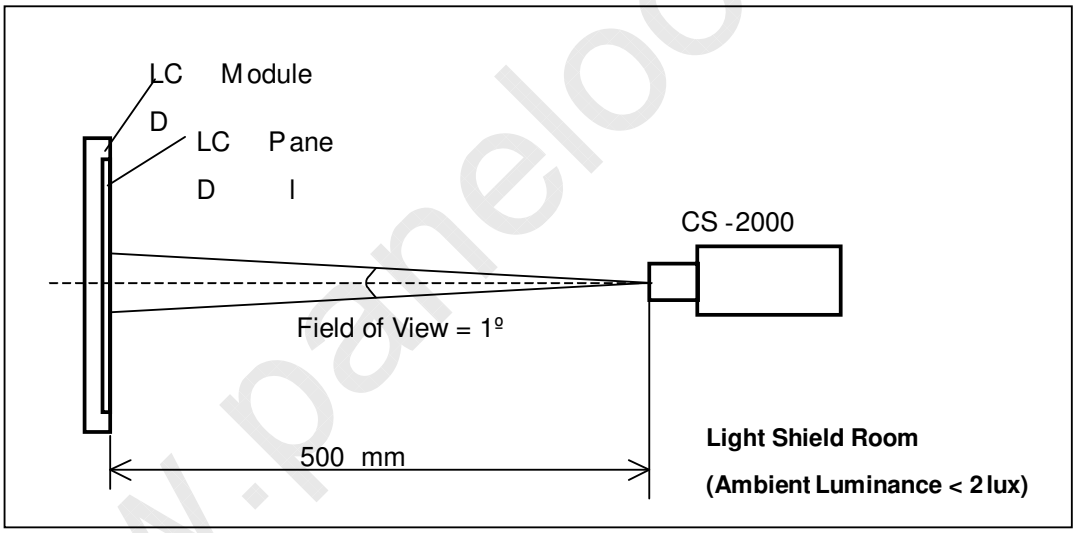
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	10.5±0.3	mA
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	4000	5000	-	-	Note (2)
Response Time		Gray to gray		-	5.5	10	ms	Note (3)
Center Luminance of White		LC		400	500	-	cd/m^2	Note (4)
White Variation		δW		-	-	(1.3)	-	Note (6)
Cross Talk		CT		-	-	(4)	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.635	Typ. +0.03	-	-
		Ry			0.323		-	
	Green	Gx			0.288		-	
		Gy			0.600		-	
	Blue	Bx			0.148		-	
		By			0.050		-	
	White	Wx			0.280		-	
		Wy			0.285		-	
	Color Gamut	C.G		68	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	Note (1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Conoscope Cono-80

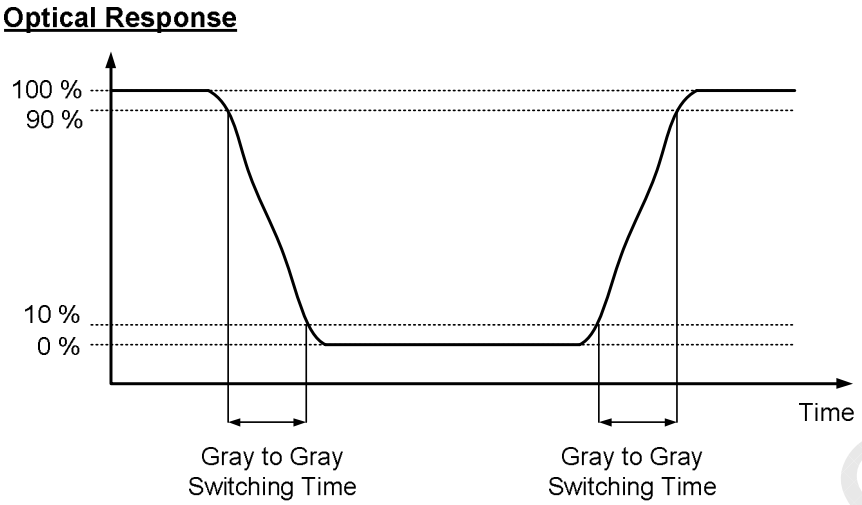
Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

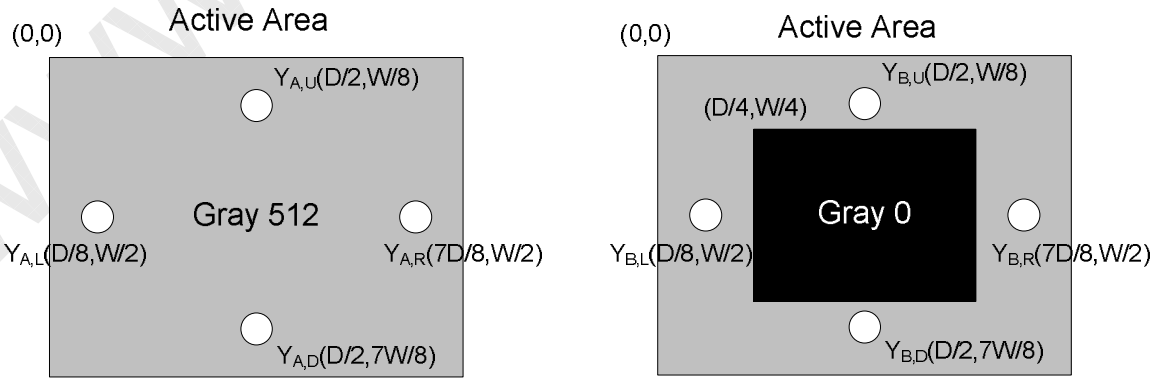
Note (5) Definition of Cross Talk (CT):

CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

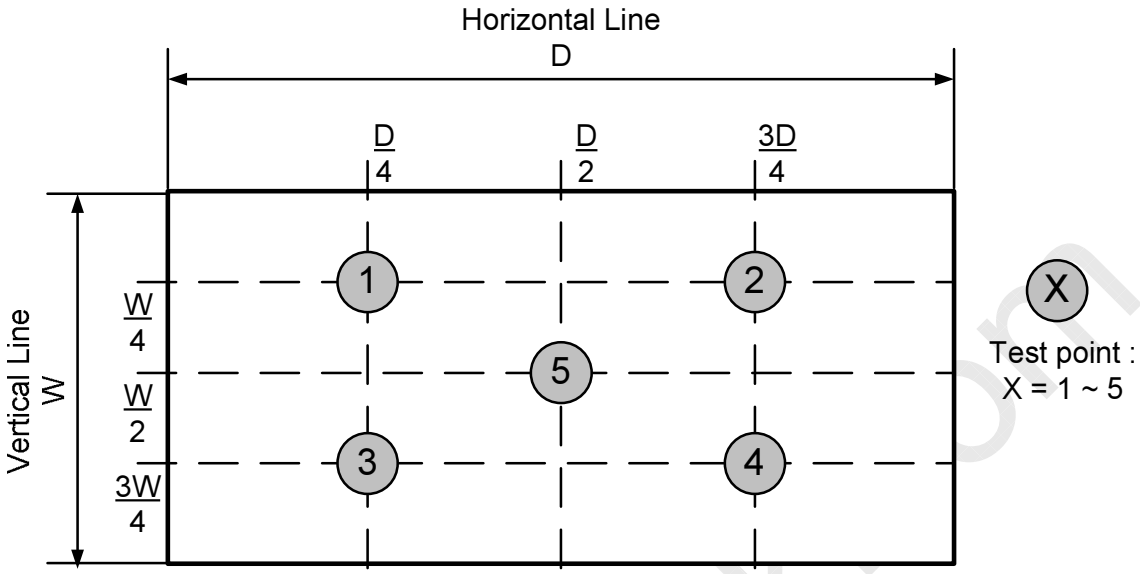
YB = Luminance of measured location with gray level 0 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

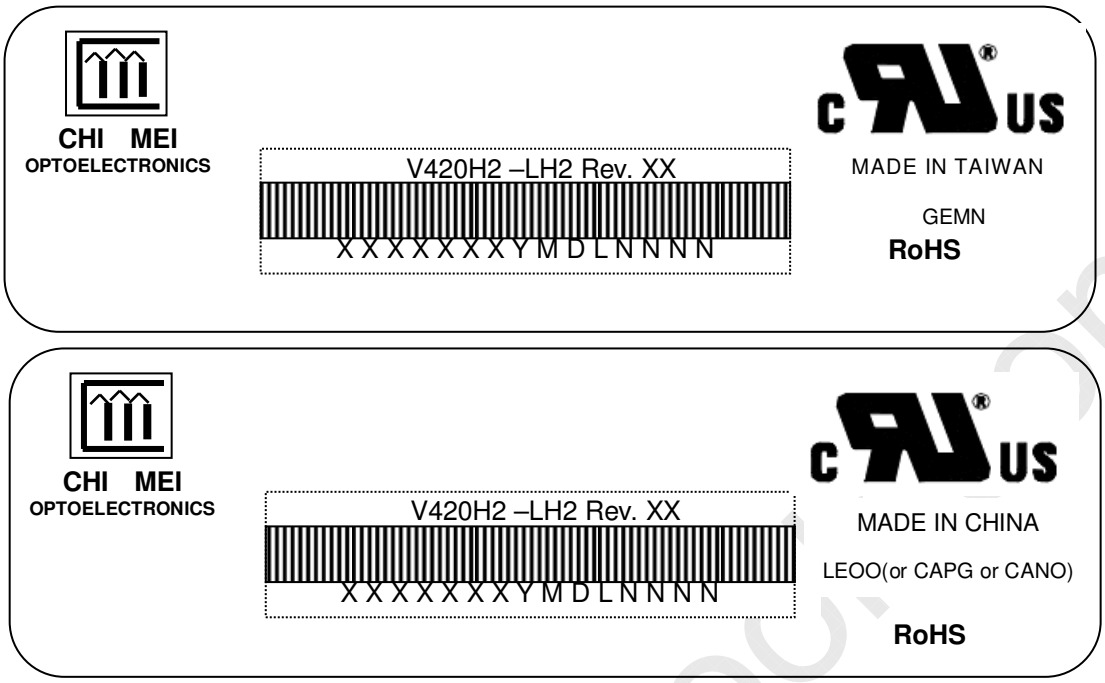
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

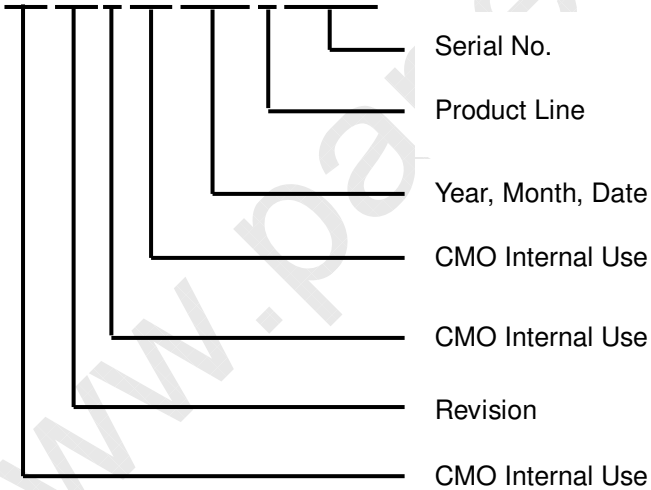
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V420H2-LH2

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month : 1~9, A~C, for Jan. ~ Dec.

Day : 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 → Line1, 2 → Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions : 1085(L)x296(W)x653(H)mm

(3) Weight : Approx. 53.17Kg(4 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

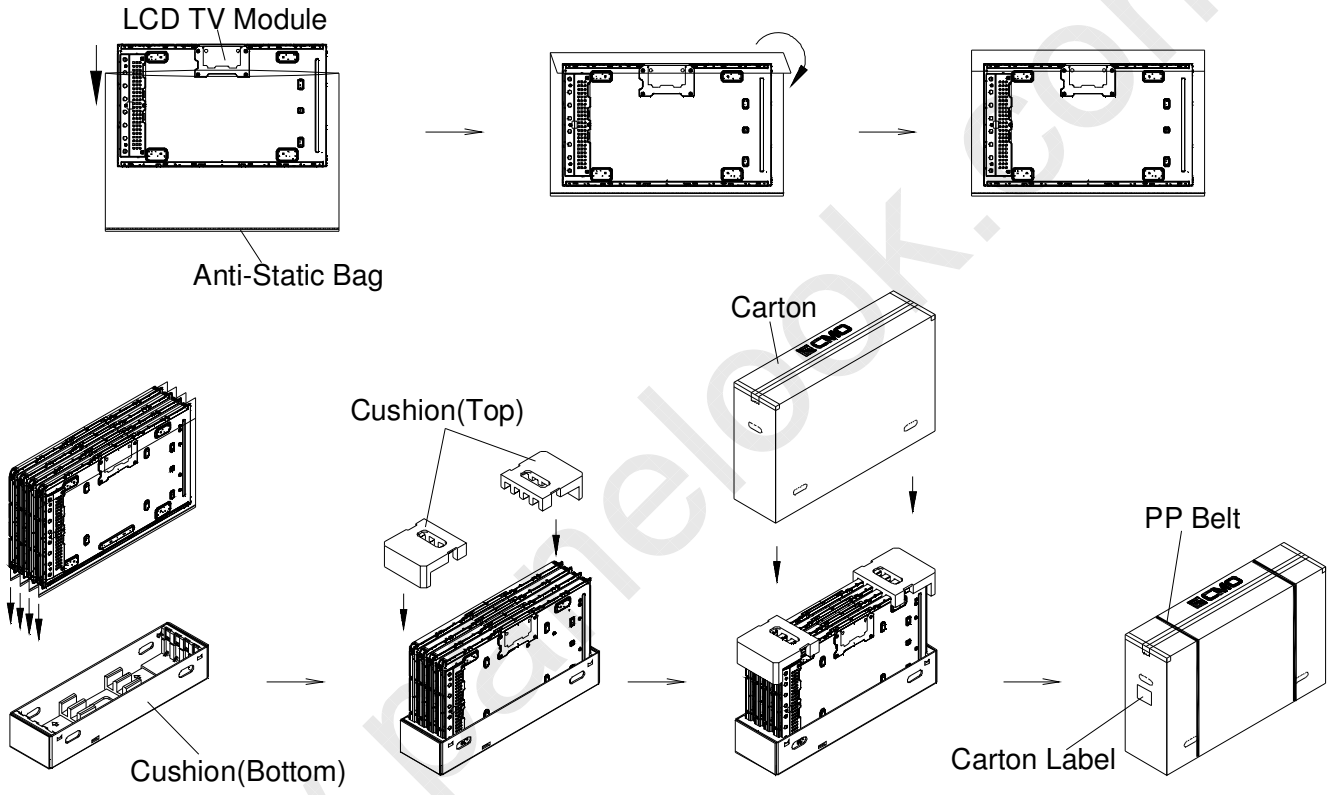
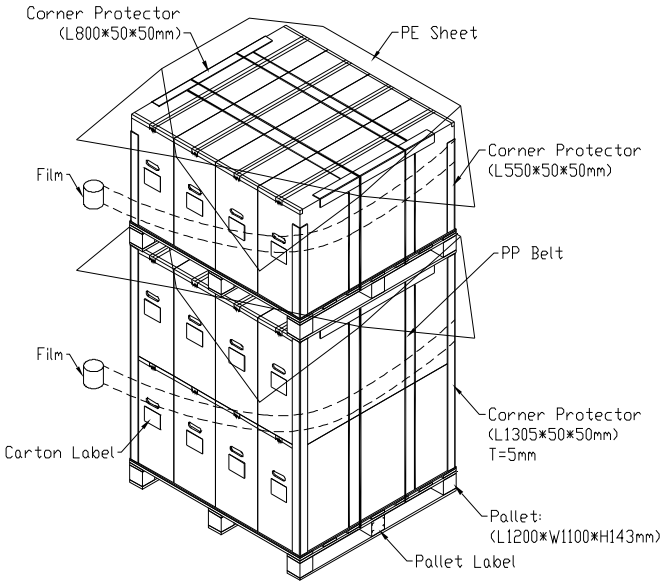


Figure 10-1 packing method

Sea / Land Transportation
(40ft Container)



Air Transportation

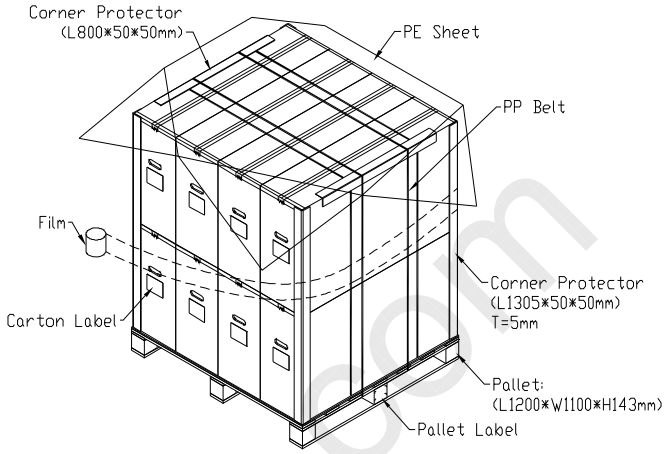


Figure 10-2 packing method

11. MECHANICAL CHARACTERISTIC